SUBSTITUTE SPECIFICATION

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TITLE OF THE INVENTION

TEST STRUCTURE FOR ELECTRICALLY VERIFYING THE DEPTHS OF TRENCH-ETCHINGS IN AN SOI WAFER, AND ASSOCIATED WORKING METHODS

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TEST STRUCTURE FOR ELECTRICALLY VERIFYING THE DEPTHS OF TRENCH-ETCHINGS IN AN SOI WAFER, AND ASSOCIATED WORKING METHODS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001]   The invention relates to a test structure and methods for verifying of isolation trench-etchings (trench etchings) in SOI wafers.

2. Description of Background and Other Information

[0002]   For integrating logic elements at a low voltage level and high voltage power elements into the same silicon circuit it is necessary to insulate die regions having significantly differing potentials from each other. One option is the dielectric insulation using etched re-filled trenches (trench isolation). To this end a vertically acting insulation between the device and the substrate is realized by means of a buried (horizontal) insulating layer (typically comprised of silicon dioxide, while generally other insulating layers may be used). A laterally acting insulation is obtained by etching a trench to the buried insulating layer and subsequently re-filling the deep trench with insulating layers or with a single insulating layer (isolation trench).

[0003]   Alternatively, only a portion of the etched trench may be filled with the insulating material. The remaining portion is filled with a conductive fill layer comprising, for instance, polysilicon. By a subsequent planarization, a so-called planarization step, for instance, an appropriate etch process or a chemical mechanical polishing (CMP) process, a planarization of the surface is accomplished, in this respect refer to the representation in FIG. 3 (prior art).

[0004]   In known techniques various problems may arise with respect to the depth. In order to achieve electric insulation in the lateral direction, that is, from one insulated island to a adjacent insulated island, it has to be guaranteed that the isolation trench extends to the buried oxide. A typical conventional technique is hereby pushed to its physical limits. An endpoint detection based on the etch composition of the etch plasma (oxygen ions are present within the etch plasma when the buried oxide layer is reached) fails when the fraction of the area etched is too small.

[0005] Optical techniques are becoming increasingly difficult, when the aspect ratio, i.e., the ratio of width and depth, is too small, that is, for narrow deep trenches.

[0006] On the other hand, etching too long causes, due to back scattering of etch ions, an etch attack at the lower sidewalls of the etched trenches and should be avoided if possible.

[0007] Additionally, in view of a desirably high tool throughput during. the manufacturing of SOI wafers including logic devices and power devices the etch time may not be extensively long.

SUMMARY OF THE INVENTION

[0008] The present invention provides a reliable method easy to be handled in order to determine the point in time when isolation trenches are fully etched to the buried insulating layer. Hereby, the technological reliability of the etching of these trenches should be enhanced, defective products avoided and costs reduced. Alternatively, the present invention may enable the verification of the depth of trenches obtained during an etch process by means of a test structure without requiring the precise measurement of the depth.

[0009] Pursuant to the foregoing, present invention includes a test structure. A row of connected islands is configured such that each island is surrounded by a trench after the etch process. The trench has a step-wise different width from one island to the other, thereby including a width used in the active circuit. The surrounding trench of each island shares a portion with the trench of the adjacent island. This portion (or section) has a different width, which is the width of the trench having the next larger or the next smaller measure in the row.

[0010] The respective common section of the trenches of the respective adjacent (downwardly) island has the measure of width of the next narrower trench. The respective common section of the trenches of the respective adjacent (upwardly) island has the measure of width of the next broader trench. Also, a mixture of different widths along the row of trenches may be set via the mask (may be prepared by means of a mask).

[0011] Under most conditions the etch rate depends to a certain degree on the width of the trenches to be etched. The broader the trench the better is an exchange of the etch species and the higher is the etch rate. Hence, based on an appropriate process control and an appropriate

layout of the widths, respectively, the broader trenches are already fully etched (to the buried insulating layer), while the narrower trenches or the narrow trenches are not yet completely etched down to the buried insulating layer.

[0012] By means of an electric measurement between two adjacent islands across the common isolation trench (disposed in between) testing and controlling may be performed with respect to a sufficiently deep etching. The measurement of the "electric pass" may include the conductivity, the resistance or the resulting current caused by a fixed voltage or the resulting voltage caused by a fixed current. All of these items represent a technical type of electric pass.

[0013] With a still insufficient depth of the etching process, i.e., when the respective isolation trench has not yet reached the buried insulating layer, a current flow increased by some orders of magnitude or a reduced resistance may be observed compared to an already sufficient depth of the etched trench having already reached the buried insulating layer.

[0014] The conductivity or the resistance are measured successively between the individual islands, starting with the islands of the narrowest trench and/or between a respective island and the surrounding region of the semiconductor substrate, for example. In this way, it may be determined which of the isolation trenches is already etched through (down to the buried insulating layer) and which is trench is not.

[0015] By means of such a test structure a deep etching may be tested whether the trenches completely etched (all trenches having a width greater than the trench of the active circuit that is indicated as a reference trench) and also the reference trench itself are etched down to the insulating layer. The remaining trenches, i.e., the trenches having a width less than the reference trench are not completely etched, thus not yet reaching the buried insulating layer.

[0016] In this manner unduly long etch times may be avoided. These undue etch times would occur if the trenches formed with a smaller width compared to the reference trench would completely be etched.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017]   The invention will be explained and supplemented by means of an illustrative embodiment, whereby.

- FIG. 1a schematically depicts a test structure in a top view.
- FIG. 1b is a cross-sectional view of the test structure of FIG. 1a, wherein isolation trenches are already present after a certain etch time.
- FIG. 2 represents the electric measurement from one island to another across a test trench illustrated in a enlarged view that is not yet completely etch and that has an aspect ratio of z/y (width to depth).
- FIG. 3 represents a trench in an active circuit in the SOI.

DETAILED DESCRIPTION OF THE INVENTION

[0018]   FIGS. 1a and 1b illustrate as a top view and a cross-sectional view, respectively, a row of continuous square-shaped island regions A to E. The perimeters of the island regions indicate the isolation trenches 16 to 20 having a different width after the etch process. The trench widths a to e between the individual islands increase from island A to island E. Hence, the etch rate also increases corresponding to the trenches formed. The etch rate $\Delta y/\Delta t$ is set in advance by means of the width z of the opening of a mask.

[0019]   An insulating layer 1 is formed, for instance, as silicon dioxide, and supports the active semiconductor layer 2. This semiconductor may be, for example, silicon. A carrier substrate below the insulating layer 1 is indicated in dotted lines. The insulating layer then represents a BOX layer (buried oxide). In FIG. 3, it is referred to in a symbolic manner.

[0020]   Each of the islands is surrounded by trenches. Each trench has a different width, and the width of the trenches a to e, which is generally represented by z, increases from left to right in FIGS. 1a, 1b, that is, z = a to e, where, e>d, d>c, c>b, etc. (from right to left).

[0021]   The remaining substrate region surrounding the trenches or the islands is denoted as S.

[0022]   The widths of the trenches 16 to 21 in FIG. 1b are indicated in the cross-sectional representation as a to e, where e is greater than a.

[0023]   A section of an isolation trench already filled and disposed in a carrier substrate is illustrated in FIG. 3 as a "handle wafer". This configuration is per se known and is merely explained here in order to provide an exemplary illustration for the reference trench or the width, that is, the depth of the reference trench resulting from the etching process of the active circuit.

[0024]   The handle wafer comprises a carrier substrate 3, a buried insulating layer 1 in the form of a BOX, which may be silicon dioxide, and an active silicon layer 2. The active layer is also frequently referred to as a "device wafer" or device substrate. In this device wafer is provided a trench structure 8 in the form of an insulation trench (isolation trench) having two insulating layers 4 provided laterally at the left and right sides and having an initial width d for an insulation. The left and right regions 6 and 7, both of which may be active silicon areas and which may be at different potentials, for example, a high voltage for a power device and a control voltage for this power device, respectively, are insulated. The vertical insulation is provided by the BOX, the horizontal insulation is provided by the two insulating layers 4. They are filled in between with a possibly conductive fill layer 5 and extend to the BOX layer.

[0025]   The surface of the device is planarized by means of a removal or a polishing process.

[0026]   Illustrated is the depth of the trench structure having a width d, which is not yet provided with the insulating layers 4 and the fill layer 5 and which extends down to the BOX such that the horizontal insulation cooperates via the insulating layers provided at this time with the vertical insulation (the BOX layer 1) so as to commonly provide a horizontal-vertical insulation. The regions 6 and 7 are completely insulated from each other. The insulation corresponds to the resistance against break-through (thickness and construction) of the insulating layers 4 and 1.

[0027]   The test structure of FIG. 1a in a top view enables the testing of the etchings of the isolation trenches with respect to, for instance, the described trench configuration 8 according to FIG. 3. The test structure is located at a different position of the SOI substrate.

[0028]   At the non-etched state, FIG. 1a may define the mask openings, which subsequently will result in etch depths that will have a configuration after the predefined etch time as is illustrated in the cross-sectional view of FIG. 1b.

[0029]   Here, two etch depths should be described, which may be recognized on the basis of the heights h16 and h2. The thickness of the device wafer h2 is reduced within the trenches 19, 20 and 21 down to the BOX layer 1. Thus, this etch depth is h2. The etch depth in the narrower trench 16 surrounding the island A is h16. There remains a bottom web h2 - h16 of the device wafer, as is the case for the step-wise broader trenches 17 and 18 having the widths b and c, respectively.

[0030]   The continuous row of islands A to E are associated with each other and are separated by a trench. Thus, they are continuous in the sense that they are functionally associated, wherein, however, each island is separated from the other island by at least one trench section. In the case of square-shaped islands, one square-shaped trench surrounds a respective island and one section of the one island and a different section of the next trench of the next island represent a common portion.

[0031]   Since each island is surrounded by a trench of different width the commonly shared section of the trench may have a width that either corresponds to the width of the broader trench or to the width of the narrower trench. The width of the respective trench increases from the left to the right in FIG. 1a. The commonly shared section between respective two adjacent islands is here dimensioned such that the broader trench separates the adjacent islands, that is, the trench width b separates the islands A and B, although island A only has the trench width a as a separation from the remaining substrate region S. Thus, the substrate region S surrounds island A at three sides, while surrounding island B only at two sides. Both cases represent an at least partial surrounding of each island with respect to the substrate region S.

[0032]   It is evident that the broadest trench width "e" is already obtained between the islands D and E so that the right trench section having the numeral z (generally used for the trench width) is no longer broader compared to the left trench section e located between the islands D and E.

[0033]   The width increases step-wise from the left to the right for each island. A section of the trench surrounding a respective island comprises the part described above that is commonly shared with the neighboring island. This respective part has a width corresponding to the width of the trench of the (right) neighboring island, when viewed from the right to left in FIG. 1a. A

consideration and usage from the right to the left is also possible. In this case, the trench located between the islands D and E has the smaller width, i.e., the width "d" of that trench that surrounds the island D. Then, the trench section between the islands A and B has the width a and not the width b.

[0034] For the inner islands B to D that are not located at the end of the series (islands A and E) the trench width in the commonly shared trench section is thus determined either by the respective one or the adjacent trench width.

[0035] One of the widths a to e corresponds, at least substantially, to a trench width of the active circuit, in this example the trench width d of the (still unfilled and laterally not yet insulated) trench structure 8 of FIG. 3. Thus, trench 19 is obtained as a reference trench that also has the width d. When etched down to the oxide layer 1 during the etch process, this also corresponds an appropriate etch depth in the active circuit between the islands 6, 7 to be insulated in the active "device substrate".

[0036] In a method for testing the isolation trench structure the test structure according to FIG. 1a may be used, after the etch process the test structure according FIG. 1b may be used. It is formed on the process wafer and the electric resistance may be measured between each two adjacent islands according to FIG. 2, in order to obtain an assessment of the sufficient or appropriate depth of the etched isolation trenches relating to active "device substrate" by means of the magnitude of the values (measurement values).

[0037] FIG. 2 illustrates in this respect two electrodes, which are symbolically applied to two island regions. These two islands are adjacent to each other and are separated by a trench. It may be each of the trenches in FIG. 1a and each of the pairs of islands that are adjacent to each other. The resistance across the electrodes resulting between these two islands is measured. The electric pass in the form of either current, resistance or conductance, or the conductivity behavior at a fixed drive current and measured voltage across the electrodes, yields measurement values. These measurement values relate to the remaining thickness of the "device substrate" under the trenches already etched and having the depth y, whereby y is a function of time, $y(t)$, and the rate with which the depth of the trench is etched is a function of the width z. The depth y of the

trench is thus a function of z, that is, $y = y(z)$. The resulting measurement values of the pass, for instance, the resistance, demonstrate which trench is already etched down to the oxide layer. The trench 19 would result in a very high resistance for a measurement between the islands C and D, while a measurement between the islands A and B, that is, across the remaining fin below the trench 17, would result in a significantly smaller resistance for the electric measurement.

[0038]   The electric measurement is performed successively, that is, for all adjacent pairs of islands, not necessarily subsequently, however, not simultaneously for all adjacent islands.

[0039]   Instead of measuring between two adjacent islands the measurement may be performed between a respective island and the substrate surface, which surrounds the respective island at least at two or three sides.

[0040]   The measurement may be performed after an etch process in order to obtain information about the used time period of the etch process and the achieved result by electrically measuring the test structure.   The etch process may also be interrupted after an etch step to allow a measurement and to monitor the progress of the etch process.   Both aspects result in the performance of the testing of the etching of the isolation trenches and that it is ensured that the complete etching is achieved, while not using an unduly long etch time period.   A subsequent measurement of the trench depth in the active region is also achieved by means of the test structure.

[0041]   In an alternative test structure, which is not explicitly illustrated, all of the continuous island regions A to E are bordered at the outer side with respect to the substrate region S by a trench width corresponding to at least the width e of the broadest trench.   In this way, each of the islands is separated from the remaining substrate region S in an early stage so that the common sections between the respective islands, that is, the widths a to e, are only available for the control measurements.   During the etching or a step of the etch process a frame-like separation of the individual islands from the substrate region at an early stage is achieved by a fast etching down of the broadest trench and a subsequent staged successive etching of the remaining trench sections of step-wise narrower width between the individual islands.

[0042]   The illustrated coordination (mapping) of the trench width of the trench 19 corresponding substantially to the width of the trench structure 8 (without the insulating layer 5 and fill layer 4) of FIG. 3, is substantially located in a central position of all trench widths of FIG. 1a.

[0043]   The tests in view of an appropriate trench depth are performed in a non-destroying manner, and after the formation of the trench structure no further processing steps are necessary that involve the wafer and the manufacturing processes of the wafer.

[0044]   With respect to the electric measurement, a high accuracy of the resistance measurement may not be required, after the dimensions of the depth of the trench and the residual fin are to be measured, rather, an interpretation is required for obtaining a possible threshold.   A very high and characteristic resistance value, representing an isolation trench etched down to the oxide layer, is to be distinguished from a low resistance obtained when a residual fin is still remaining. The determination of this may be accomplished in an efficient and rapid manner.